WHAT IS CLAIMED IS:

1. An apparatus including a decision feedback equalizer with dynamic feedback control for adaptively controlling a pre-slicer data signal that is sliced to provide a post-slicer data signal, comprising:

first signal combining circuitry that combines a feedback signal and an input signal representing a plurality of data to provide a pre-slicer signal;

signal slicing circuitry, coupled to said first signal combining circuitry, that slices said pre-slicer signal to produce a post-slicer signal indicative of said plurality of data;

decision feedback circuitry including input signal timing control, coupled to said signal slicing circuitry, that feeds back said post-slicer signal in response to a control signal to produce said feedback signal;

second signal combining circuitry, coupled to said signal slicing circuitry, that combines said pre-slicer and post-slicer signals to produce a difference signal indicative of a difference between said pre-slicer and post-slicer signals;

signal differentiation circuitry with a selected signal delay that differentiates and delays said input signal to produce a resultant signal, wherein respective portions of said differentiated signal are delayed relative to corresponding portions of said input signal by said selected signal delay; and

third signal combining circuitry, coupled to said second signal combining circuitry and said signal differentiation circuitry, that combines said difference signal and said resultant signal to produce said control signal, wherein said selected signal delay is selected such that said control signal has a substantially zero AC signal component.

2. The apparatus of claim 1, wherein said first signal combining circuitry comprises a signal summing circuit.

3. The apparatus of claim 1, wherein said signal slicing circuitry comprises a voltage comparison circuit.

4. The apparatus of claim 1, wherein said decision feedback circuitry comprises:

signal timing control circuitry, coupled to said signal slicing circuitry, that selectively delays said post-slicer signal in response to said control signal to produce a delayed post-slicer signal; and

feedback filter circuitry, coupled to said signal timing control circuitry, that filters said delayed post-slicer signal to produce said feedback signal.

5. The apparatus of claim 1, wherein said decision feedback circuitry comprises:

signal timing control circuitry, coupled to said signal slicing circuitry, that selectively delays said post-slicer signal in response to said control signal to produce a delayed post-slicer signal;

tapped delay circuitry, coupled to said signal timing control circuitry, that successively delays said delayed post-slicer signal to produce a plurality of further delayed post-slicer signals;

mixer circuitry, coupled to said tapped delay circuitry, that mixes each one of said plurality of further delayed post-slicer signals with a respective one of a plurality of coefficient signals to produce a plurality of mixed signals; and

fourth signal combining circuitry, coupled to said mixer circuitry, that combines said plurality of mixed signals to produce said feedback signal.

6. The apparatus of claim 1, wherein said second signal combining circuitry comprises a signal summing circuit.

7. The apparatus of claim 1, wherein said signal differentiation circuitry comprises high pass filter circuitry that high pass filters and delays said input signal to produce said resultant signal.

8. The apparatus of claim 1, wherein said signal differentiation circuitry comprises:

a high pass filter circuit that high pass filters said input signal to produce a high pass filtered signal; and

signal delay circuitry, coupled to said high pass filter circuit, delays said high pass filtered signal to produce said resultant signal.

9. The apparatus of claim 1, wherein said third signal combining circuitry comprises:

a signal multiplication circuit that multiplies said difference signal and said differentiated signal to produce a product signal; and

low pass filter circuitry, coupled to said signal multiplication circuit, that low pass filters said product signal to produce said control signal.

10. The apparatus of claim 1, wherein said third signal combining circuitry comprises:

a signal multiplication circuit that multiplies said difference signal and said differentiated signal to produce a product signal; and

signal integration circuitry, coupled to said signal multiplication circuit, that integrates said product signal to produce said control signal.

11. An apparatus including a decision feedback equalizer with dynamic feedback control for adaptively controlling a pre-slicer data signal that is sliced to provide a post-slicer data signal, comprising:

first signal combiner means for combining a feedback signal and an input signal representing a plurality of data and generating a pre-slicer signal;

signal slicer means for slicing said pre-slicer signal and generating a post-slicer signal indicative of said plurality of data;

decision feedback means for controlling signal timing by feeding back said post-slicer signal in response to a control signal and generating said feedback signal;

second signal combiner means for combining said pre-slicer and post-slicer signals and generating a difference signal indicative of a difference between said pre-slicer and post-slicer signals;

signal differentiator means with a selected signal delay for differentiating and delaying said input signal and generating a resultant signal, wherein respective portions of said differentiated signal are delayed relative to corresponding portions of said input signal by said selected signal delay; and

third signal combiner means for combining said difference signal and said resultant signal and generating said control signal, wherein said selected signal delay is selected such that said control signal has a substantially zero AC signal component.

12. A method for providing decision feedback equalization with dynamic feedback control for adaptively controlling a pre-slicer data signal that is sliced to provide a post-slicer data signal, comprising:

combining a feedback signal and an input signal representing a plurality of data and generating a pre-slicer signal;

slicing said pre-slicer signal and generating a post-slicer signal indicative of said plurality of data;

feeding back said post-slicer signal with controlled signal timing in response to a control signal and generating said feedback signal;

combining said pre-slicer and post-slicer signals and generating a difference signal indicative of a difference between said pre-slicer and post-slicer signals;

differentiating and delaying said input signal and generating a resultant signal, wherein respective portions of said differentiated signal are delayed relative to corresponding portions of said input signal by a selected signal delay; and

combining said difference signal and said resultant signal and generating said control signal, wherein said selected signal delay is selected such that said control signal has a substantially zero AC signal component.

13. The method of claim 12, wherein said feeding back said post-slicer signal with controlled signal timing in response to a control signal and generating said feedback signal comprises:

selectively delaying said post-slicer signal in response to said control signal and generating a delayed post-slicer signal; and

filtering said delayed post-slicer signal and generating said feedback signal.

14. The method of claim 12, wherein said feeding back said post-slicer signal with controlled signal timing in response to a control signal and generating said feedback signal comprises:

selectively delaying said post-slicer signal in response to said control signal and generating a delayed post-slicer signal;

successively delaying said delayed post-slicer signal and generating a plurality of further delayed post-slicer signals;

mixing each one of said plurality of further delayed post-slicer signals with a respective one of a plurality of coefficient signals and generating a plurality of mixed signals; and

combining said plurality of mixed signals and generating said feedback signal.

15. The method of claim 12, wherein said differentiating and delaying said input signal and generating a resultant signal comprises:

high pass filtering said input signal and generating a high pass filtered signal; and

delaying said high pass filtered signal and generating said resultant signal.

16. The method of claim 12, wherein said combining said difference signal and said resultant signal and generating said control signal comprises:

multiplying said difference signal and said differentiated signal and generating a product signal; and

low pass filtering said product signal and generating said control signal.

17. The method of claim 12, wherein said combining said difference signal and said resultant signal and generating said control signal comprises:

multiplying said difference signal and said differentiated signal and generating a product signal; and

integrating said product signal and generating said control signal.